PUSH-PULL CLASS-AB TRANSFORMERLESS POWER AMPLIFIERS *

By Larry Blaser and Heitor Franco

SUMMARY

One of the major problems in power amplifier design is to combine high efficiency with thermal stability. Class-C operation with current drive is one possibility but distortion level is high due to cross-over and nonlinearity of h_{FE}. A new diode compensation method is described which allows high efficiency Class-AB operation for maximum output and lowest distortion; and with excellent thermal stability. In the output stage the variation of the quiescent current versus temperature is kept small by a diode-resistance network in the emitter of each driver transistor; thereby eliminating the need for large thermal compensating resistance in the emitters of the output transistors.

A 10-watt amplifier was designed using the described power dissipation criteria and the new biasing scheme. Performance of the amplifier demonstrates the effectiveness of the design. It operates with maximum power dissipation up to 65°C ambient with a sine wave input. Calculations are also included in the paper which show the voltage levels of maximum power dissipation for sine, triangular and square waves.

I. INTRODUCTION

This paper discusses general problems in connection with dissipation, distortion, and thermal stability of transistor power amplifiers. A comparison of distortion between Class-C and Class-AB operation with current and voltage drives shows the advantages of Class-AB operation. A new bias scheme is presented to solve the problem of thermal instability. The results of the Class-AB amplifier analysis, summarized in Section II, can generally be applied to the design of most transistor power amplifiers.

A 10-watt push-pull Class-AB transformerless audio power amplifier was built as a typical application of the design principles presented. Performance of this amplifier is given and its circuit described in Section V.

II. GENERAL DESIGN CONSIDERATIONS OF PUSH-PULL POWER AMPLIFIERS

In a power amplifier, high efficiency requires operation in Class AB, B, or C.

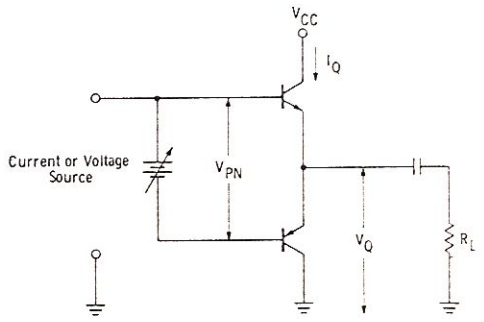

FIG. 1. Push-pull power gain stage of complementary emitter followers.

For the analysis of power dissipation of the push-pull circuit shown in Fig. 1, let:

V_{CC} = supply voltage
V_Q = emitter quiescent voltage
V_{PN} = voltage between the two bases of the transistors
I_Q = quiescent current (zero for Class B or C)
R_L = load resistance

In the case where $V_Q = V_{CC}/2$ and $I_Q = 0$, the maximum power dissipation in each output transistor, which occurs at other than maximum power output, is given by:

$$P_{Dmax} \simeq K_D \frac{V_{CC}^2}{R_L} \qquad (2.1)$$

where K_D is a coefficient given in Table I for three common waveforms.

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This maximum power dissipation should never exceed the permissible dissipation P_P:

$$P_{Dmax} \leq P_P \qquad (2.2)$$

The permissible dissipation can be expressed by:

$$P_P = \frac{T_{Jmax} - T_A}{\theta_{J-C} + \theta_{C-A}} \qquad (2.3)$$

where

T_A = ambient air temperature

T_{Jmax} = maximum permissible junction temperature

θ_{J-C} = thermal resistance between the junction and the case of the transistor

θ_{C-A} = thermal resistance between the case of the transistor and the ambient air.

According to equation (2.1), for a given load resistance, R_L, the maximum power dissipation per output transistor depends only on the supply voltage, V_{CC}. In order not to exceed the permissible dissipation, the following relation must be satisfied:

$$V_{CC} \leq \sqrt{\frac{R_L P_P}{K_D}}$$

$$V_{CC} \leq K_C \sqrt{R_L P_P} \qquad (2.4)$$

where

$$K_C = \frac{1}{\sqrt{K_D}} \quad \text{(see Table I)}$$

The maximum power output, P_{Omax}, of a transistor power amplifier is given by:

$$P_{Omax} = K_O \frac{\left(V_{CC} - 2V_{CE(min)}\right)^2}{R_L} \qquad (2.5)$$

where

$V_{CC} - 2V_{CE(min)}$ = maximum peak-to-peak output voltage

$V_{CE(min)}$ = minimum collector-to-emitter on voltage at maximum output current

K_O = factor given in Table I for sine, triangular, and square waves

TABLE I

	Sine Wave	Triangular Wave	Square Wave
K_D	$\frac{1}{4\pi^2}$	0.0235	$\frac{1}{32}$
K_C	2π	6.5	5.6
K_O	$\frac{1}{8}$	$\frac{1}{12}$	$\frac{1}{4}$

In Section VI (appendix), the relation (2.1) giving the maximum power dissipation per output transistor is derived for a sine wave in the general case of $V_Q \neq V_{CC}/2$ and $I_Q > 0$. It is shown, however, that if I_Q is much smaller than the maximum output current over the temperature range, the contribution of the quiescent current to the power dissipation is negligible. The best efficiency is obtained when the quiescent voltage, V_Q, is one-half of the supply voltage, V_{CC}. If this is not the case, the power dissipation is given by the relations (6.11), (6.21), and (6.28) of Section VI instead of by equation (2.1).

Two other problems in connection with the power dissipation, for which there are several approaches, are cross-over distortion and thermal instability. If the output is operated in Class C, there is no quiescent current and thus no thermal instability. The resultant distortion can be reduced by driving the output stage from a current source and by applying large feedback over the amplifier; but for reasons which will be presented in Section III, cross-over distortion may still be a problem. If, as an alternative, the output transistors are operated in Class AB to eliminate cross-over distortion, then thermal stability must be considered.

In a Class-AB output stage, temperature sensitive elements such as diodes or thermistors are

commonly used in the biasing network in conjunction with a resistor in each emitter. However, this type of temperature compensation is not completely effective for transient temperature changes due to power dissipation of the output transistors. Therefore, a sufficient factor of safety in this circuit requires an emitter resistance which is not small compared with the load resistance, thus reducing the amplifier efficiency. A biasing scheme which allows safe operation in Class AB without sacrificing the efficiency or the maximum power output capability is described in Section IV.

III. DISTORTION IN PUSH-PULL TRANSISTOR AMPLIFIERS

Distortion in Class AB and C push-pull transistor amplifiers will be analyzed using Fig. 2, which is a simplified schematic of a complementary emitter follower circuit.

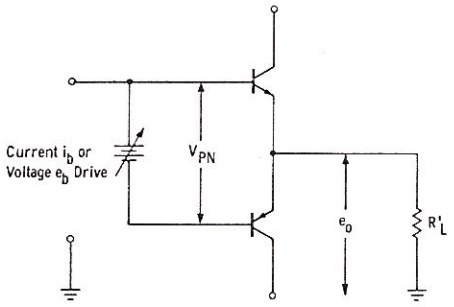


FIG. 2. Simplified complementary emitter-follower stage.

First, consider the voltage V_{PN} to be zero. In this case the amplifier will operate in Class C. A voltage source drive will give the cross-over distortion shown in Fig. 3 due to nonconduction of both transistors during the period from $(\pi/2 - \alpha)$ to $(\pi/2 + \alpha)$. Outside of this region the output signal will be:

$$e_o = e_b - V_{BE} \qquad (3.1)$$

where

V_{BE} = Voltage drop from base to emitter when the transistor is on.

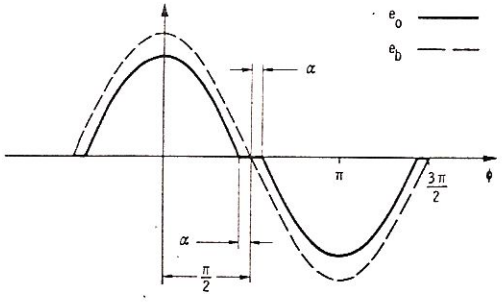


FIG. 3. Cross-over distortion waveform with voltage drive.

The variations of V_{BE} are negligible outside of the region $(\pi/2 - \alpha)$ to $(\pi/2 + \alpha)$ hence during the conduction period the output signal is simply a portion of a sine wave.

A current source drive will result in the output waveform shown in Fig. 4. The waveform includes two types of distortion. The nonlinearity of the I_C/I_B transfer function shown in Fig. 5 causes one type of distortion. There is also a cross-over distortion that can be explained as follows: when the current i_b changes sign, there will be no output current until the base emitter capacitance changes to the V_{BE} (on) voltage.

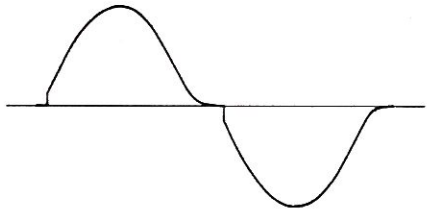


FIG. 4. Cross-over distortion waveform with current drive.

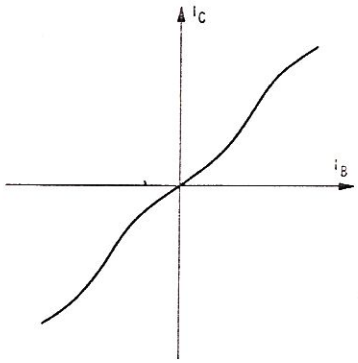


FIG. 5. I_C/I_B characteristic showing the nonlinearity due to h_{FE} variations with I_B or I_C.

In Class-AB operation the voltage V_{PN} is adjusted so that the transistors draw a small quiescent current. With the conduction angle greater than π and a voltage source drive, distortion will result only from variations in V_{BE} (on) which are negligible during the conduction period, as was already mentioned. However, with a current source drive, there would be no great advantage over the Class-C operation because even though the cross-over distortion would disappear, there is no appreciable improvement of the I_C/I_B characteristic. The advantages of Class-AB operation are thus evident for voltage drive if a reliable bias scheme, such as discussed in detail in Section IV, is used to control quiescent current.

The output waveform in Class AB with a voltage source drive and a quiescent current equal to 1% of the peak a-c current is compared with the input voltage in Fig. 6. (Voltage scales for the two waveforms are slightly different.)

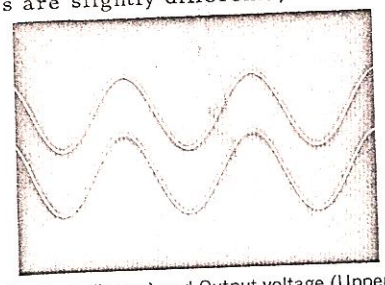


FIG. 6. Input voltage (Lower) and Output voltage (Upper) in Class AB at $I_Q = 1\%$ I_P, $I_P = 100$ mA; frequency 1 kc.

IV. BIASING AND D-C STABILITY OF A CLASS-AB OUTPUT STAGE

The new biasing method which stabilizes the Class-AB output stage is shown in Fig. 7. The complementary phase inverter, Q_3 and Q_4, is included in the biasing network.

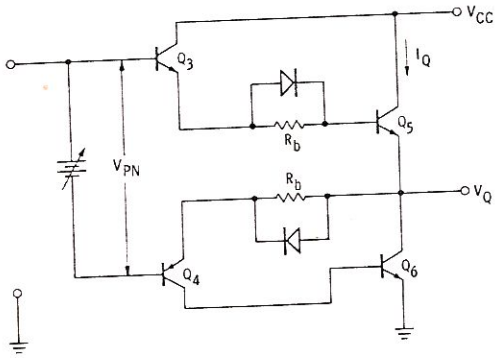


FIG. 7. Output section of amplifier with resistance diode bias network.

In the analysis of the variations of I_Q as a function of V_{PN} and of the temperature, T, first assume R_b equals zero. The voltage V_{PN} will then be equal to the sum of the V_{BE}'s of the transistors Q_3, Q_4 and Q_5, and will have an I_Q/V_{PN} idealized characteristic as shown in Fig. 8. This

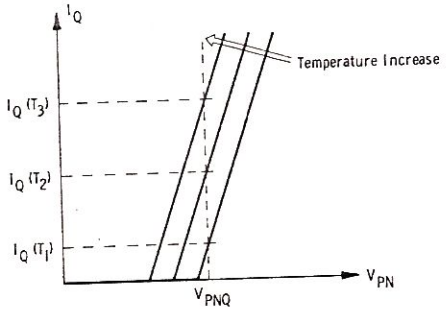


FIG. 8. Idealized characteristic of I_Q/V_{PN}.

characteristic is given for three different temperatures, T_1, T_2, and T_3, to show that a small variation of temperature will produce a large change in the current I_Q.

There is, therefore, an unstable condition since an increase in I_Q produces an increase in the dissipation of Q_5 and subsequently a rise in temperature which tends to raise I_Q.

The V_{BE} of a transistor varies with junction temperature, T_J. This variation can be caused by both ambient temperature changes and transistor power dissipation. The ambient temperature effect is compensated by making V_{PN} equal to the forward drop, V_{PNQ}, of three diodes which, in series, track the variation of the I_Q/V_{PN} characteristic.

The dissipations in the transistors Q_3 and Q_4 are negligible. Only the dissipation in Q_5, which can raise the temperature of this junction well above the ambient, has to be taken into account. It will cause the I_Q/V_{PN} characteristic to shift to the left, producing an excessive increase in I_Q and possibly thermal runaway.

Secondly in this analysis, the resistance R_b is made greater than zero; and this resistance shunted by diodes, as shown in Fig. 7, results in the I_Q/V_{PN} characteristic of Fig. 9.

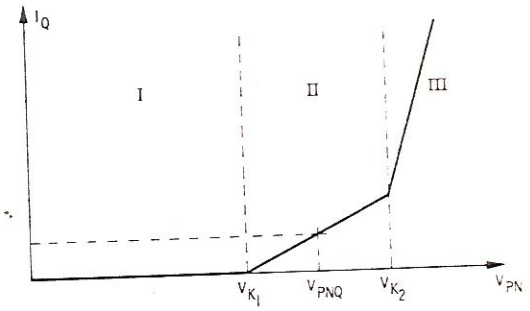


FIG. 9. New I_Q/V_{PN} characteristic resulting from the insertion of the resistance diode network.

The voltage V_{PN} across the three diodes in series should fall in region II of the characteristic. The difference $(V_{PNQ} - V_{K_1})$ should be independent of temperature, but unfortunately the compensation is not perfect and a slight variation occurs (V_{K_1} decreases faster than V_{PNQ} for increasing temperature).

The width of region II decreases with increasing temperature since it is determined by two diodes in series. Besides these variations, it is necessary to consider the variations of the temperature of Q_5 due to power dissipation. The junction temperature of Q_5 can rise well above the ambient tem-

perature which will cause the (I_Q/V_{PN}) characteristic to shift to the left. At the same time, the current gain of Q_5 increases. For $R_b > 500\,\Omega$ the base current of Q_5 is practically independent of temperature.

The following procedure can be used to obtain the value of I_Q. In Fig. 10, let:

T_A = ambient temperature
ΔT = increase of temperature of Q_5
$h_{FE}(T)$ = d-c current gain of Q_5 at the temperature T

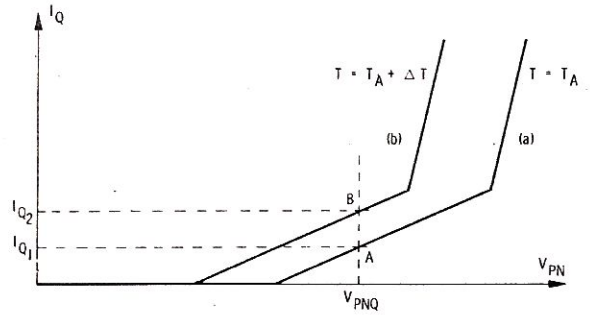


FIG. 10. Shift of the I_Q/V_{PN} characteristic due to temperature increase.

Curve (a) in Fig. 10 shows the I_Q/V_{PN} characteristic at ambient temperature, T_A, and curve (b) shows the same characteristic shifted by the effect of ΔT. At the ambient temperature, the quiescent current is I_{Q_1} — point A, curve (a). At a higher temperature, $T_A + \Delta T$, the curve is shifted by ΔT such that the new quiescent current is I_{Q_2} — point B, curve (b). The quantity for ΔV is given by the expression:

$$\Delta V \simeq -2\,\Delta T \quad (mV/°C)$$

where

-2 mV/°C = the temperature coefficient of the characteristic (a).

In calculating I_{Q_2} it has been assumed that $h_{FE}(T_A + \Delta T)$ of Q_5 is equal to $h_{FE}(T_A)$. However, the h_{FE} of Q_5 does vary with T; therefore, to obtain I_{Q_3} at $T_A + \Delta T$, I_{Q_2} must be multiplied by a correction factor ϵ.

$$\epsilon = \left.\frac{h_{FE}(T_A + \Delta T)}{h_{FE}(T_A)}\right|_{I_Q = I_{Q_3}} \qquad (4.1)$$

and

$$I_{Q_3} = \epsilon I_{Q_2} \qquad (4.2)$$

Since ϵ is a function of I_{Q_3}, a trial and error method must be used to obtain the correct value. R_b is chosen to satisfy the requirement that,

$$I_{Q_3} \ll \frac{V_{CC} - V_Q}{R_L} \qquad (4.3)$$

For example:

$$I_{Q_3} < 0.05\,\frac{V_{CC} - V_Q}{R_L}$$

V. A 10-WATT AUDIO AMPLIFIER

The circuit shown in Fig. 11 is a variation of the basic design(*) used in most transformerless transistor power amplifiers. The emitter-follower stage Q_1 provides a high input impedance to the amplifier. Common-emitter stage Q_2 supplies the d-c bias for the output section by means of the three diodes D_1, D_2 and D_3. They are in series with the collector resistance which is bootstrapped to increase the available voltage swing beyond the power supply voltage, V_{CC}. Complementary emitter followers Q_3 and Q_4 (see Fig. 2) in Class AB provide a low impedance drive to the load $R_L' \simeq h_{FE} R_L$. However, NPN power transistors Q_5 and Q_6 are necessary to supply the output current required into the load, R_L. The gain is given by: (See appendix in Section VI.)

$$A \simeq -\frac{Y_s}{Y_f} \simeq -\frac{R_f}{R_s}$$

The series resistor-capacitor combination, R_1C_1, at the amplifier output corrects the phase of the feedback at high frequency for the inductive load offered by a loudspeaker. The R_2C_2 network, paralled with R_f, and the capacitor C_3, connected from base to collector of Q_2, provide a controlled roll-off at 60 kc. D-c feedback is applied through the base-bias resistance of Q_2 which stabilizes the amplifier for temperature variations. The biasing adjustment in the base of Q_2 is set for V_Q (d-c voltage at the emitter of Q_5) to be equal to $V_{CC}/2$. Therefore, the formulas of Section II can be applied. Because the amplifier is intended for sound reproduction, the coefficients in Table I for the case of a sine wave will be used.

*"Quasi-Complementary Transistor Amplifier" by H. C. Lin, Electronics, September, 1956.

Amplifier Design

a. Calculation of the permissible dissipation with the following conditions:

T_A = 25°C
T_{Jmax} = 200°C
θ_{J-C} = 35°C/W — for the 2N2297 transistor
θ_{C-A} = 15°C/W — for a single-sided aluminum radiator with an approximate surface area of 100 cm^2.

Using equation (2.3)

$$P_P = \frac{T_{Jmax} - T_A}{\theta_{J-C} + \theta_{C-A}} = 3.5 \text{ W}$$

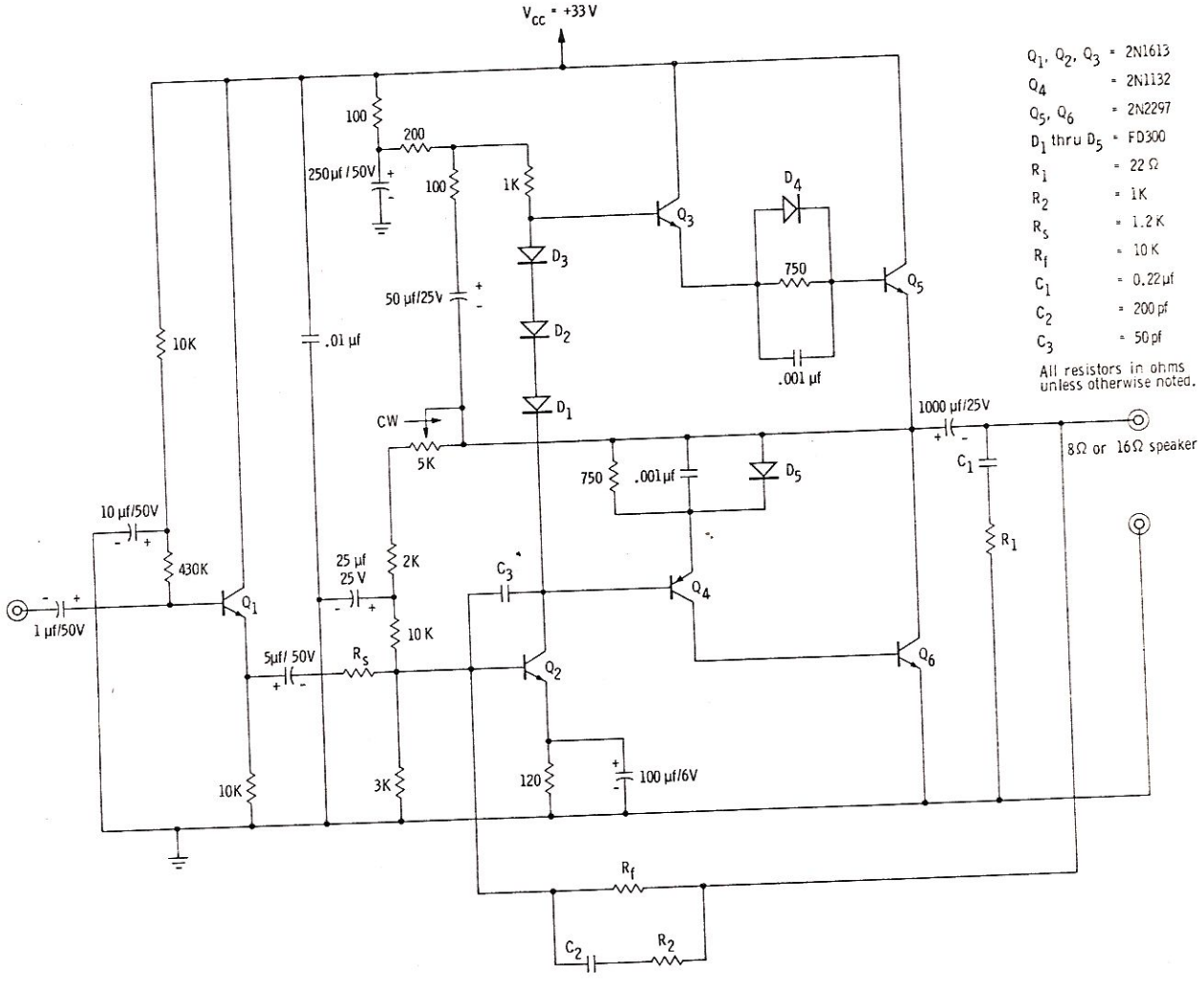
b. Calculation of the supply voltage with the following conditions:

$R_L = 8\,\Omega \quad P_P = 3.5 \text{ W} \quad K_C = 2\pi$

Using equation (2.4)

$$V_{CC} \leq K_C \sqrt{R_L P_P} = 33 \text{ V}$$

FIG. 11. 10 WATT AUDIO POWER AMPLIFIER



c. Calculation of the maximum power output with the following conditions:

$R_L = 8\ \Omega$
$V_{CC} = 33\ V$
$V_{CE}(min) = 4\ V^*$
$K_O = 1/8$

Using equation (2.5)

$$P_{Omax} = K_O \frac{\left(V_{CC} - 2V_{CE}(min)\right)^2}{R_L} = 9.8\ W$$

Amplifier Performance

a. In Fig. 12, the solid line represents the amplifier frequency response at 1-watt power output into an 8-ohm speaker load, and the dashed line represents the response at the same power output into an 8-ohm resistive load with networks R_1C_1, R_2C_2, and C_3 removed.

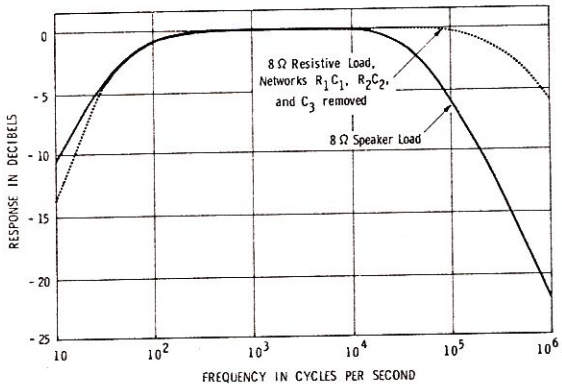


FIG. 12. Amplifier frequency response.

b. The 5-kc square wave response at 5 watts power output into an 8 Ω resistive load is given in Fig. 13.

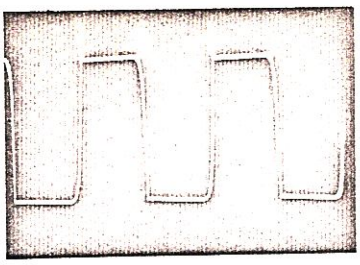


FIG. 13. Amplifier 5 kc square wave response.

c. The 1-kc harmonic distortion at 5 watts power output is less than 1%.

d. The output impedance at 1 kc is approximately 0.5 Ω.

e. The total output noise power with the input shorted is greater than 100 db below maximum rated output.

f. The power supply current versus power output is given in Fig. 14.

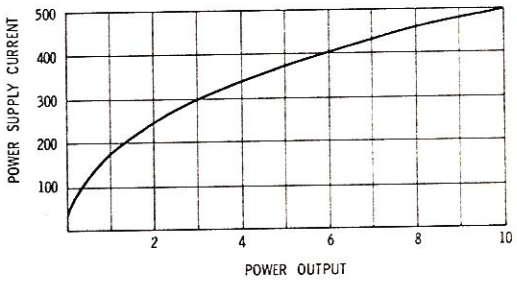


FIG. 14. Power supply current versus power output.

$$^*V_{CE}(min) = V_{BE}(on)\big|_{Q_5} + V_F\big|_{D_4} + V_{CE}(sat)\big|_{Q_3}$$

where

$V_{BE}(on)\big|_{Q_5}$ = base-to-emitter voltage drop of Q_5 at peak collector current

$V_F\big|_{D_4}$ = voltage drop across the diode D_4 at peak output current

$V_{CE}(sat)\big|_{Q_3}$ = collector-to-emitter saturation voltage of Q_3 at peak output current.

VI. APPENDIX

A. ANALYSIS OF THE POWER DISSIPATION IN THE OUTPUT TRANSISTORS

Figure 15 represents the push-pull output stage used in this analysis.

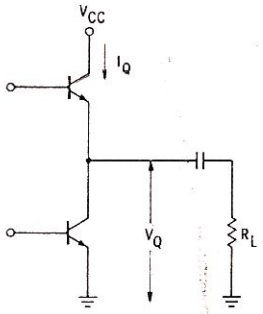


FIG. 15. Output stage of NPN power transistors.

In this analysis, let

V_{CC} = power supply voltage
V_Q = quiescent voltage with no a-c signal
I_Q = quiescent current with no a-c signal
I = rms value of output current
V = rms value of output voltage

1. Sine Wave

For a sine wave the expressions of the collector current, I_C, and collector-to-emitter voltage, V_{CE}, of Fig. 15 are:

$$I_C = I_Q + \sqrt{2}I\cos\phi \qquad (6.1)$$

$$V_{CE} = V_{CC} - V_Q - \sqrt{2}V\cos\phi \qquad (6.2)$$

The average power dissipation in the upper transistor(*) is:

$$P = \frac{1}{2\pi} \cdot 2\int_0^{\phi_0} I_C V_{CE}\, d\phi \qquad (6.3)$$

where ϕ_0 is defined as the angle at which $I_C = 0$ (see Fig. 16).

*The lower transistor is not considered because it has no influence on the d-c stability considerations of Section IV.

Hence from equation (6.1),

$$I_C = 0 = I_Q + \sqrt{2}I\cos\phi_0$$

$$\phi_0 = \frac{\pi}{2} + \arcsin\left(\frac{I_Q}{\sqrt{2}I}\right) = \frac{\pi}{2} + \Delta\phi \qquad (6.4)$$

and

$$\Delta\phi = \arcsin\frac{I_Q}{\sqrt{2}I} \qquad (6.5)$$

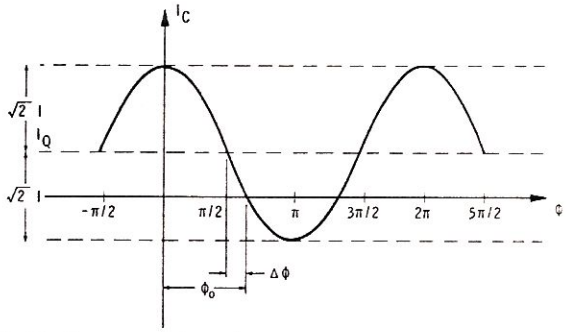


FIG. 16. Current waveform of one output transistor in Class AB operation.

From equations (6.1), (6.2), and (6.3),

$$P = \frac{1}{\pi}\int_0^{\phi_0} (I_Q + \sqrt{2}I\cos\phi)(V_{CC} - V_Q - \sqrt{2}V\cos\phi)\, d\phi \qquad (6.6)$$

$$P = \frac{1}{\pi}(V_{CC} - V_Q) I_Q \int_0^{\pi/2+\Delta\phi} d\phi + \frac{\sqrt{2}}{\pi}\left[I(V_{CC} - V_Q) - VI_Q\right]\int_0^{\pi/2+\Delta\phi} \cos\phi\, d\phi - \frac{2}{\pi} VI \int_0^{\pi/2+\Delta\phi} \cos^2\phi\, d\phi$$

$$P = \frac{1}{\pi}(V_{CC} - V_Q) I_Q \left(\frac{\pi}{2} + \Delta\phi\right) + \frac{\sqrt{2}}{\pi}\left[I(V_{CC} - V_Q) - VI_Q\right]\cos\Delta\phi - \frac{1}{\pi} VI\left(\frac{\pi}{2} + \Delta\phi - \sin\Delta\phi\cos\Delta\phi\right) \qquad (6.7)$$

Assuming that $\Delta\phi \ll \frac{\pi}{2}$ the following approximations may be made

$$\sin \Delta\phi = \Delta\phi$$

$$\cos \Delta\phi = 1$$

and replacing I by $\frac{V}{R_L}$, the average power dissipation becomes:

$$P = -\frac{V^2}{2R_L} + \frac{\sqrt{2}}{\pi} \cdot \frac{V}{R_L} (V_{CC} - V_Q - I_Q R_L) + \frac{1}{2} I_Q (V_{CC} - V_Q) \quad (6.8)$$

Differentiating with respect to V,

$$\frac{dP}{dV} = -\frac{V}{R_L} + \frac{\sqrt{2}}{\pi R_L} (V_{CC} - V_Q - I_Q R_L)$$

For

$$V = \frac{\sqrt{2}}{\pi} (V_{CC} - V_Q - I_Q R_L) = V_1, \quad (6.9)$$

$$\left.\frac{dP(V)}{dV}\right|_{V_1} = 0 \quad \text{and} \quad \frac{d^2P(V)}{dV^2} < 0$$

Therefore, V_1 corresponds to the maximum average power dissipation which has the value:

$$P(V_1) = P_{Dmax} = -\frac{1}{\pi^2 R_L} (V_{CC} - V_Q - I_Q R_L)^2 + \frac{2}{\pi^2 R_L} (V_{CC} - V_Q - I_Q R_L)^2 + \frac{1}{2} I_Q (V_{CC} - V_Q)$$

$$P_{Dmax} = \frac{1}{\pi^2 R_L} \left[(V_{CC} - V_Q)^2 - 2(V_{CC} - V_Q) I_Q R_L + I_Q^2 R_L^2\right] + \frac{1}{2} I_Q (V_{CC} - V_Q)$$

$$P_{Dmax} = \frac{1}{\pi^2} \cdot \frac{(V_{CC} - V_Q)^2}{R_L} + I_Q \left[0.3 (V_{CC} - V_Q) + \frac{I_Q R_L}{\pi^2}\right] \quad (6.10)$$

Since R_L is always small ($\leq 50\,\Omega$), for small values of I_Q the term $(I_Q R_L)/\pi^2$ may be neglected and P_{Dmax} becomes the simple expression:

$$P_{Dmax} = 0.11 \frac{(V_{CC} - V_Q)^2}{R_L} + 0.3 I_Q (V_{CC} - V_Q) \quad (6.11)$$

to justify the assumption that $\Delta\phi \ll \pi/2$ at the level $P(V_1)$, I is replaced in equation (6.5) by V_1/R_L,

$$\sin \Delta\phi = \frac{I_Q R_L}{\sqrt{2} V_1}$$

Introducing the value of V_1 from equation (6.9),

$$\sin \Delta\phi = \frac{\pi}{2} \cdot \frac{I_Q}{\frac{V_{CC} - V_Q}{R_L} - I_Q}$$

but for any practical application, the quiescent current should be much smaller than the peak current, i.e.,

$$\frac{V_{CC} - V_Q}{R_L} \gg I_Q \quad (6.12)$$

so that $\sin \Delta\phi \ll 1$ and $\sin \Delta\phi \simeq \Delta\phi$.

Under this assumption, the quiescent current I_Q has a small contribution to P_{Dmax}. The first term of equation (6.11) is the most important limitation to the power supply voltage, V_{CC}.

2. Triangle Wave

For a triangular wave, neglecting the quiescent current I_Q, (Fig. 17)

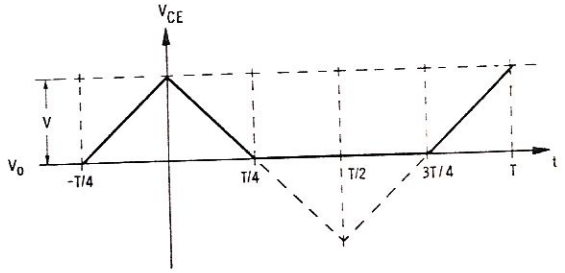


FIG. 17. Voltage waveform across one of the output transistors in Class B operation (triangular output).

$$V_{CE} = (V_{CC} - V_Q) - V\left(1 - 4\,\frac{t}{T}\right)$$

$$= V_0 - V\left(1 - 4\,\frac{t}{T}\right) \qquad (6.13)$$

$$I_C = \frac{V}{R_L}\left(1 - 4\,\frac{t}{T}\right) \qquad (6.14)$$

$$V_{CE} I_C = \frac{V_0 V}{R_L} - \frac{V^2}{R_L} + 4\,\frac{V}{R_L}\,(2V - V_0)\frac{t}{T}$$

$$- 16\,\frac{V^2}{R_L} \cdot \frac{t^2}{T^2}$$

$$= A + B\,\frac{t}{T} + C\,\frac{t^2}{T^2} \qquad (6.15)$$

$$P = \frac{2}{T}\int_0^{T/4} V_{CE} I_C\,dt = \frac{2}{T}\int_0^{T/4}\left(A + \frac{B}{T}\,t + \frac{C}{T^2}\,t^2\right)dt$$

$$= \frac{1}{2}\,A + \frac{1}{16}\,B + \frac{2}{3 \times 4^3}\,C \qquad (6.16)$$

$$P = \frac{1}{2} \cdot \frac{V}{R_L}(V_0 - V) + \frac{1}{4} \cdot \frac{V}{R_L}(2V - V_0)$$

$$- \frac{1}{6} \cdot \frac{V^2}{R_L} \qquad (6.17)$$

$$P = \frac{1}{4} \cdot \frac{V}{R_L} V_0 - \frac{1}{6} \cdot \frac{V^2}{R_L} \qquad (6.18)$$

Differentiating with respect to V ,

$$\frac{dP}{dV} = \frac{1}{4} \cdot \frac{V_0}{R_L} - \frac{1}{3} \cdot \frac{V}{R_L} \qquad (6.19)$$

For

$$V = V_1 = \frac{3}{4}\,V_0 \ , \qquad (6.20)$$

$$\left.\frac{dP}{dV}\right|_{V = V_1} = 0 \qquad \text{and} \qquad \frac{d^2P}{dV^2} < 0$$

Therefore, V_1 corresponds to the maximum power dissipation which has the value,

$$P_{Dmax} = \frac{3}{32} \cdot \frac{V_0^2}{R_L} = \frac{3}{32} \cdot \frac{(V_{CC} - V_Q)^2}{R_L} \qquad (6.21)$$

If

$$V_{CC} - V_Q = V_{CC}/2 \ ,$$

$$P_{Dmax} = \frac{3}{128} \cdot \frac{V_{CC}^2}{R_L} \qquad (6.22)$$

3. Square Wave

For a square wave, neglecting the quiescent current, I_Q , (Fig. 18)

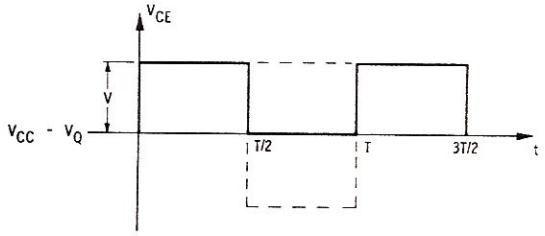


FIG. 18. Voltage waveform across one of the output transistors in Class B operation (square wave output).

$$V_{CE} = V_{CC} - V_Q - V \qquad (6.23)$$

$$I_C = \frac{V}{R_L} \qquad (6.24)$$

$$P = \frac{1}{2} \cdot V_{CE} I_C = \frac{1}{2}\left[\frac{V_{CC} - V_Q}{R_L} V - \frac{V^2}{R_L}\right] \qquad (6.25)$$

Differentiating power with respect to V ,

$$\frac{dP}{dV} = \frac{1}{2} \cdot \frac{V_{CC} - V_Q}{R_L} - \frac{V}{R_L} \qquad (6.26)$$

$$\frac{dP}{dV} = 0 \quad \text{gives} \quad V = \frac{V_{CC} - V_Q}{2} \tag{6.27}$$

and therefore

$$P_{Dmax} = \frac{1}{8} \cdot \frac{(V_{CC} - V_Q)^2}{R_L} \tag{6.28}$$

If

$$V_{CC} - V_Q = V_{CC}/2 \quad ,$$

$$P_{Dmax} = \frac{1}{32} \cdot \frac{V_{CC}^2}{R_L} \tag{6.29}$$

B. DERIVATION OF AMPLIFIER GAIN EQUATION

A general feedback amplifier is shown in Fig. 19; Y_i is the input admittance of the amplifying device, Y_L is the load admittance, A_V is the voltage gain of the device and Y_f and Y_s are the gain determining elements.

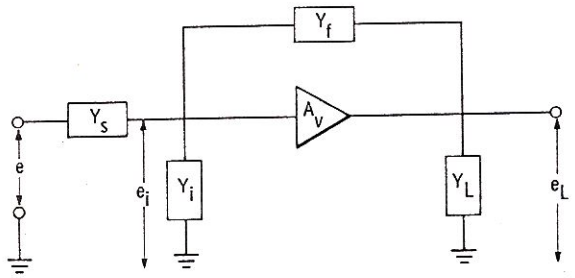


FIG. 19. General feedback amplifier.

The equations representing the amplifier are:

$$(e - e_i)\,Y_S + (e_L - e_i)\,Y_f - e_i\,Y_i = 0 \tag{6.30}$$

$$e_i = e_L/A_V \tag{6.31}$$

Solving equations (6.30) and (6.31)

$$e\,Y_S + e_L\,Y_f \left(1 - \frac{Y}{A_V Y_f}\right) = 0$$

where

$$Y = Y_S + Y_f + Y_i$$

Therefore:

$$A = \frac{e_L}{e} = -\frac{Y_S}{Y_f} \cdot \frac{1}{1 - \frac{Y}{A_V Y_f}} \tag{6.32}$$

If $A_V Y_f \gg Y$, equation (6.32) becomes

$$A = -\frac{Y_S}{Y_f} \tag{6.33}$$